UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,630	04/02/2004	Robert E. Cypher	5181-98801	2867

35690 7590 05/26/2006

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX 78701

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,630	CYPHER ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/05 7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-17 are in the application.

Claims 1-17 are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7,9-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US 2002/0019921).

As in claim 1, Hagersten describes a system, comprising: a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device (Hagersten's Fig 4); wherein an active device included in a node of the plurality of nodes includes a memory management unit configured to receive a virtual address generated within

that active device and to responsively output a global address identifying a coherency unit (Hagersten's Fig 3A: #312A MMU, column 9 line 55 to column 10 line 10);

wherein a portion of the global address identifies a translation function (Hagersten's Fig 3B, column 9 lines 17-32 describe the global address spaces coma/numa being mapped to different address space ranges for different sub-system #310,320,280. When in coma mode, each sub-system uses the global address with translation function information, for looking up and for translating global address space to its local coma address space);

wherein a memory subsystem included in the node is configured to perform the translation function identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit (Hagersten's Fig 3B);

wherein each active device included in the node is configured to use the portion of the global address identifying the translation function when determining whether a local copy of the coherency unit is currently stored in a cache associated with that active device (Hagerten's column 9 lines 15-45, column 10 lines 1-20, Fig 3B describes the local copy of coma address space is determined by using a portion of global address space by comparing it with local physical address space, the high order bits of global address are used for mapping global coma address space to different address spaces in different nodes, see Fig 3B).

As in claim 2, the claim recites wherein at least one bit included in the global address indicates whether the coherency unit identified by the global address is replicable in more than one of the plurality of nodes. The claim is rejected based on the same rationale as in the rejection

of claim 1. Furthermore, Hagersten's Fig 3B shows different copies of coma address spaces are replicable in different nodes #310, #320, #380.

As in claim 3, the claim recites wherein if the at least one bit included in a different global address indicates that the different global address is not replicable in more than one of the plurality of nodes, the portion of the different global address includes additional address bits instead of identifying a translation function. Hagersten's Fig 3B shows that the address space can be configured to operate in coma mode or in numa mode. If it is operated in numa mode, the address space comprises address spaces of all nodes in the system, therefore the global address bits using in the numa mode must be larger than the corresponding address bits using in the coma mode.

As in claim 4, the claim recites wherein the additional portion of the global address for the coherency unit generated by each active device in the plurality of nodes has a same value, and wherein active devices in different nodes of the plurality of nodes generate different values of the portion of the global address identifying the translation function. The claim rejected based on the same rationale as in the rejection of claim 3. Since in the numa mode, addressing are shared among nodes. Therefore the translation portion of the global address has the same values that correspond to the local physical address portion in each node (see Fig 3B).

As in claim 5, the claim recites wherein a home memory subsystem included in a home node of the plurality of nodes for the coherency unit is configured to store the portion of the global address identifying the translation function for the node, wherein active devices included in the home node are configured to generate a different value of the portion of the global address, wherein the different value identifies a different translation function associated with the

coherency unit in the home node (Hagersten's column 9 lines 1-30 describes the global address translations in coma mode for different nodes in a system. Hagersten further teaches the address translation or mapping scheme can be applied to finer granularity, in another word mapping to the processors in each node, since each node comprising four processors.

As in claim 6, the claim recites wherein if the home memory subsystem determines that the coherency transaction involving the coherency unit cannot be completed within the home node, the home memory subsystem is configured to provide the portion of the global address identifying the translation function for the node a home interface included in the home node for conveyance to the node (Haersten's Fig 3B, column 10 lines 30-40, column 10 line 11 to column 11 line 6 teaches a home node can translate and converting the global address space information to that of the owner's node and forwarding the request to the owner's node translator function).

As in claim 7, the claim recites active device included in the node is configured to output the global address in an address packet on an address network coupling the active device to an additional active device within the node in order to initiate a coherency transaction for a coherency unit identified by the global address. Hagersten's column 9 line 55 to column 10 lines 10, Fig 3C-3E shows the request will be handled by comparing if there is a valid data in the processor cache, if not the global address will be mapped and matching to local cache in the node.

Claim 9 rejected based on the same rationale as in the rejection of claim 1.

Claim 10 rejected based on the same rationale as in the rejection of claim 2.

Claim 11 rejected based on the same rationale as in the rejection of claim 3.

Claim 12 rejected based on the same rationale as in the rejection of claim 4.

Claim 13 rejected based on the same rationale as in the rejection of claim 5.

Claim 14 rejected based on the same rationale as in the rejection of claim 6.

Claim 15 rejected based on the same rationale as in the rejection of claim 7.

As in claim 16, the claim recites an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the translation lookaside buffer entry includes the global address, wherein the operating system selects the translation function in order to map the virtual address to the local physical address within a non-replicated range of local physical addresses of the memory subsystem (Hagersten's Fig 3A MMU management unit converting virtual address to physical address. Furthermore, it's well known fact that a MMU management unit includes a translation look aside buffer to maintaining frequently used translation values; It's note that the mapped physical addresses are used in both coma and numa modes, and in numa mode, the data is not replicable).

As in claim 17, the claim recites the operating system executing on the active device in one of the nodes creating the translation lookaside buffer entry corresponding to the virtual address in response to deciding to replicate the coherency unit to the node from an additional one of the plurality of nodes. The claim rejected based on the same rationale as in the rejection of claim 16. Its note that the mapped physical addresses are used in both coma and numa modes, and in coma mode, the data is replicable.

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US 2002/0019921) as applied to claim 1 and in view of Arimili et al (US 2002/0112124).

As in claim 8, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the active device. Hagersten does not describe the claim's aspect of integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Hagersten's system to allow fast communication between the processor and the memory controller since they are located in the same chip (Arimilli's page 1 paragraph 6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimilli et al (US 2003/0009640).

Weber (US 6209064).

Liberty (US 6275900).

Zahir et al (US 6604184).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 5/24/06

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER